Avispado: A RISC-V core supporting the RISC-V vector instruction set

Roger Espasa, PhD

CEO

SemiDynamics

- European Based RISC-V IP Provider
  - HQ in Barcelona
  - Founded 2016
- Proud participant in the European Processor Initiative (EPI)
  - RISC-V Acceleration core supplied by SemiDynamics

Semidynamics High Bandwidth RISC-V IP Cores

AVISPADO 220 

2-wide In-Order

Gazzillion Misses™

RISC-V Vector Support

TODAY's FOCUS

ATREVIDO 220 

2-wide Out-of-Order

Gazzillion Misses™

RISC-V Vector Support

Available for licensing

What's a high bandwidth core?

A core with lots of outstanding memory requests

A core with Gazzillion Misses™

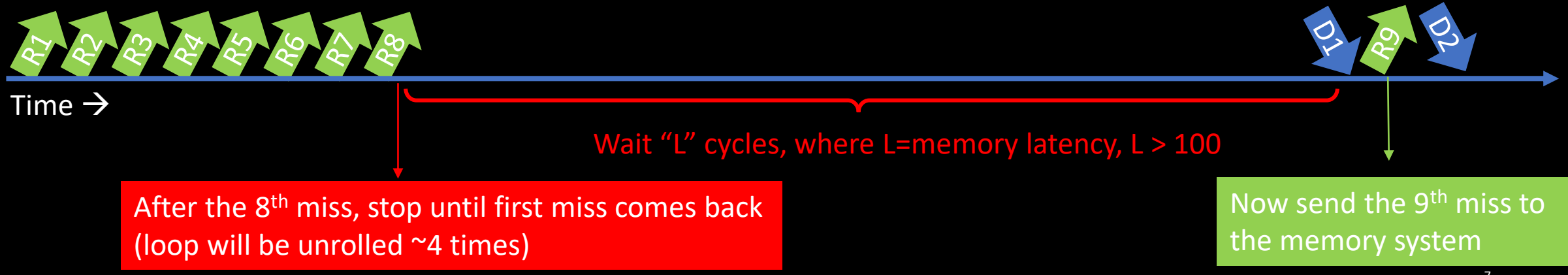
Example: Gathering Sparse Data with 8 outstanding requests

Original Program

```
while ( condition )
    load  a[index[i]]
    load  b[i]
    compute
    store c[i]
```

Stylized Assembly Code

```
top:
    load  index[i] -> x5
    load  (x5) -> x6
    load  b[i] -> x7
    compute x6, x7 -> x8
    store x8 -> c[i]
    loop to top
```



Example: Gathering Sparse Data with *Gazzillion Misses™*

Original Program

```
while ( condition )
    load  a[index[i]]
    load  b[i]
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Stylized Assembly Code

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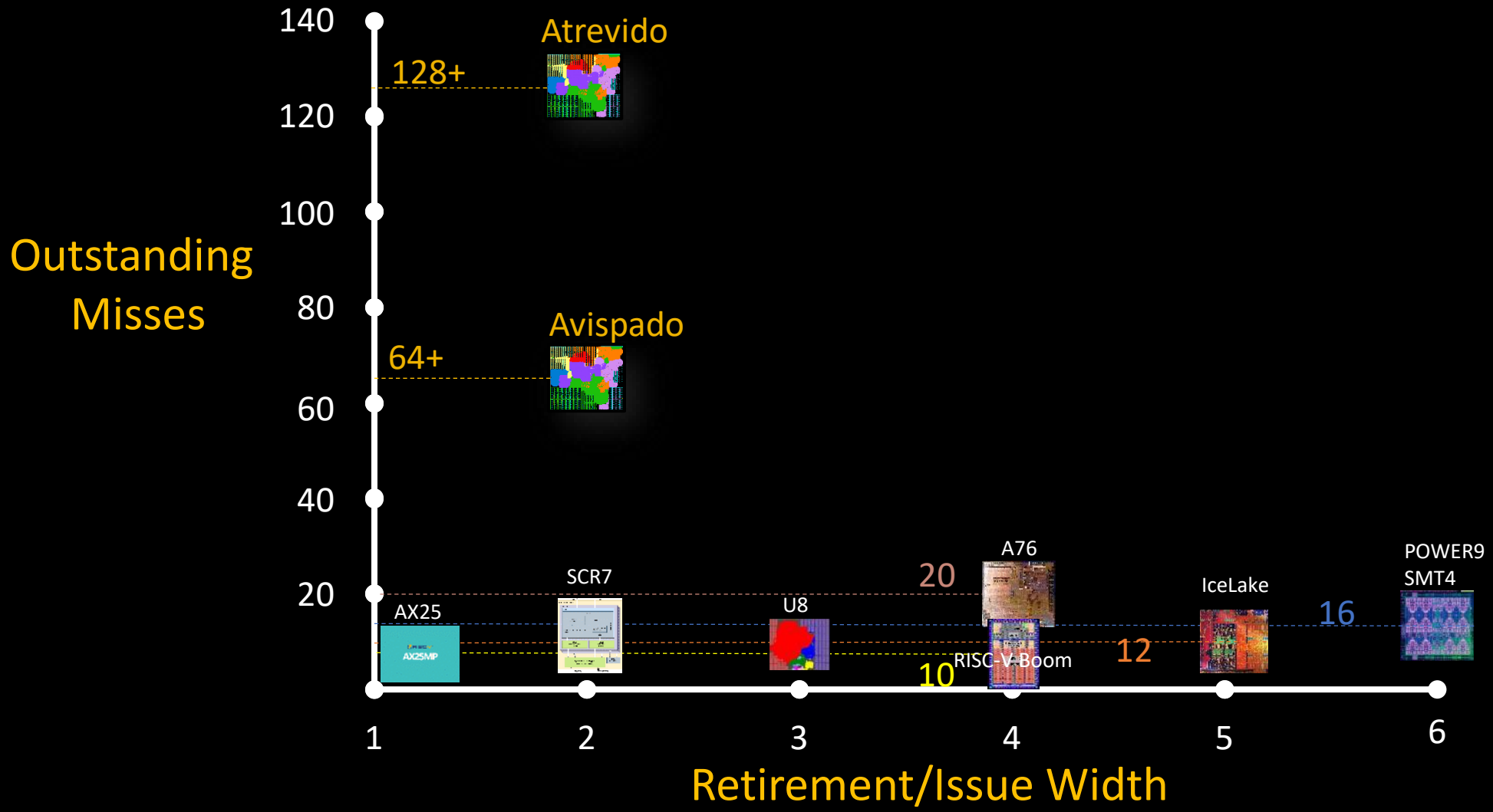
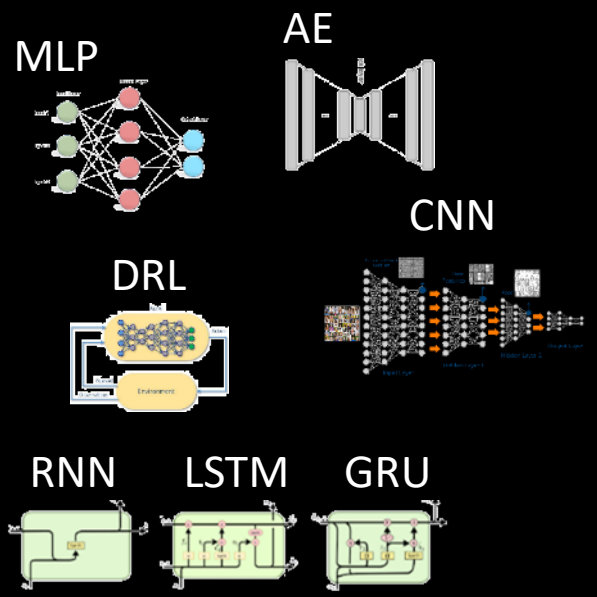
Comparison to other cores



Gazzillion Misses™ good for…

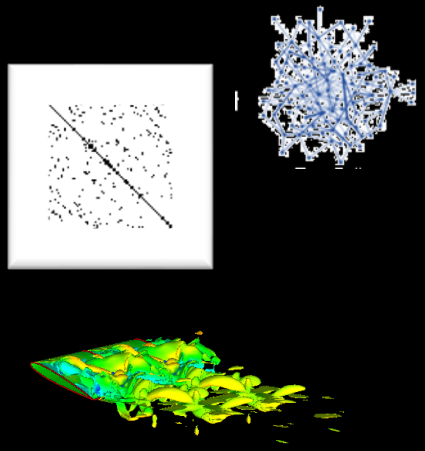
Machine Learning

Recommendation Systems



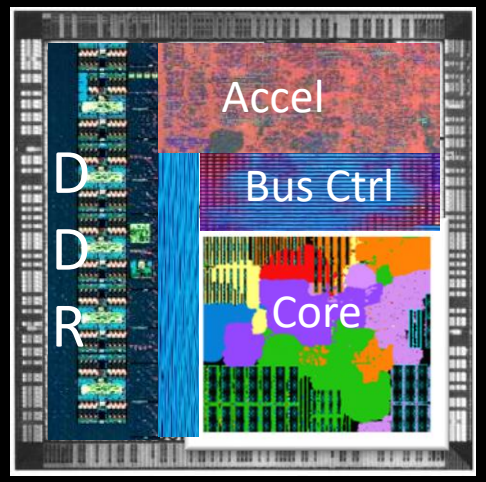
Key-Value Stores

Sparse Data / HPC

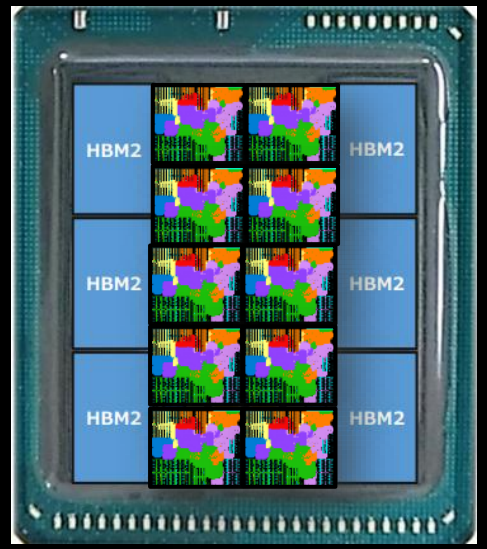


Gazzillion Misses™ good for SoCs...

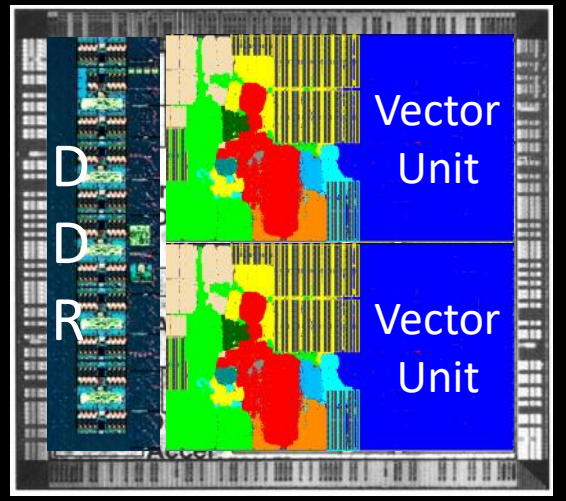
With Limited SRAM/Cache



High Bandwidth/ Streaming



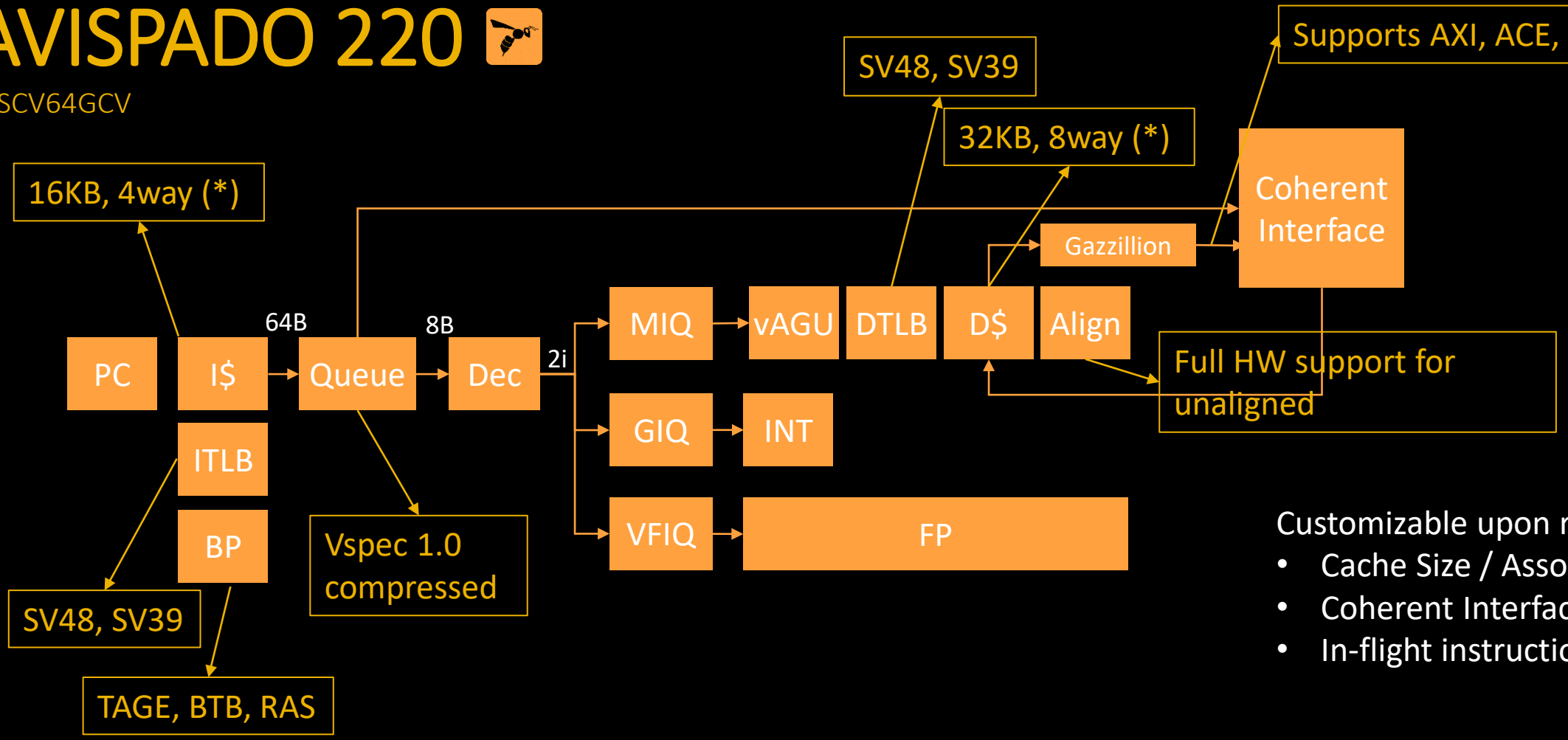
With Vector Units



Avispado Core Details

AVISPADO 220

RISCV64GCV



Customizable upon request:

- Cache Size / Associativity
- Coherent Interface
- In-flight instructions

Breakpoint support
External Debug over JTAG/DM

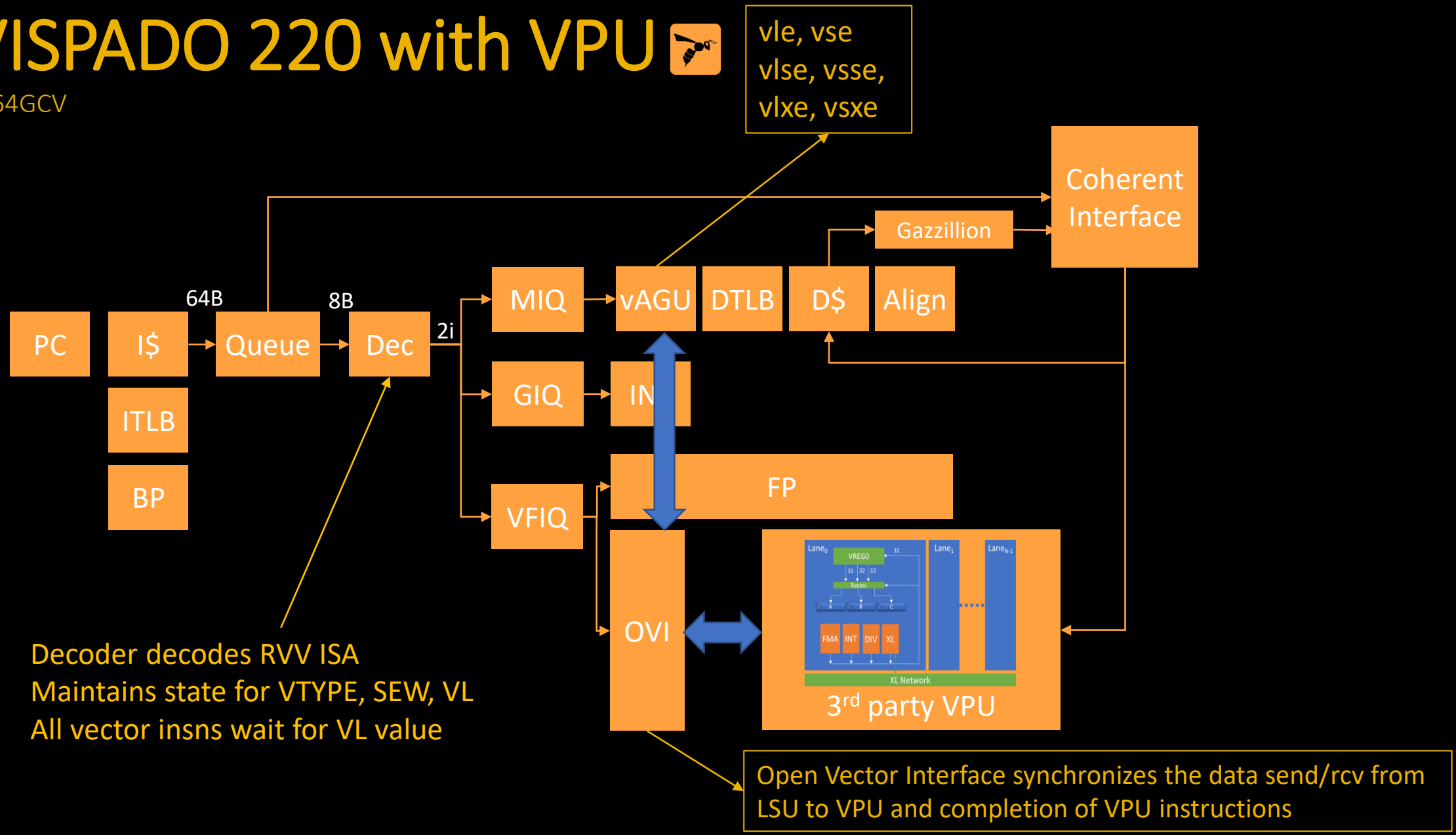
Support for RISC-V Vector Instructions

Support for RVV

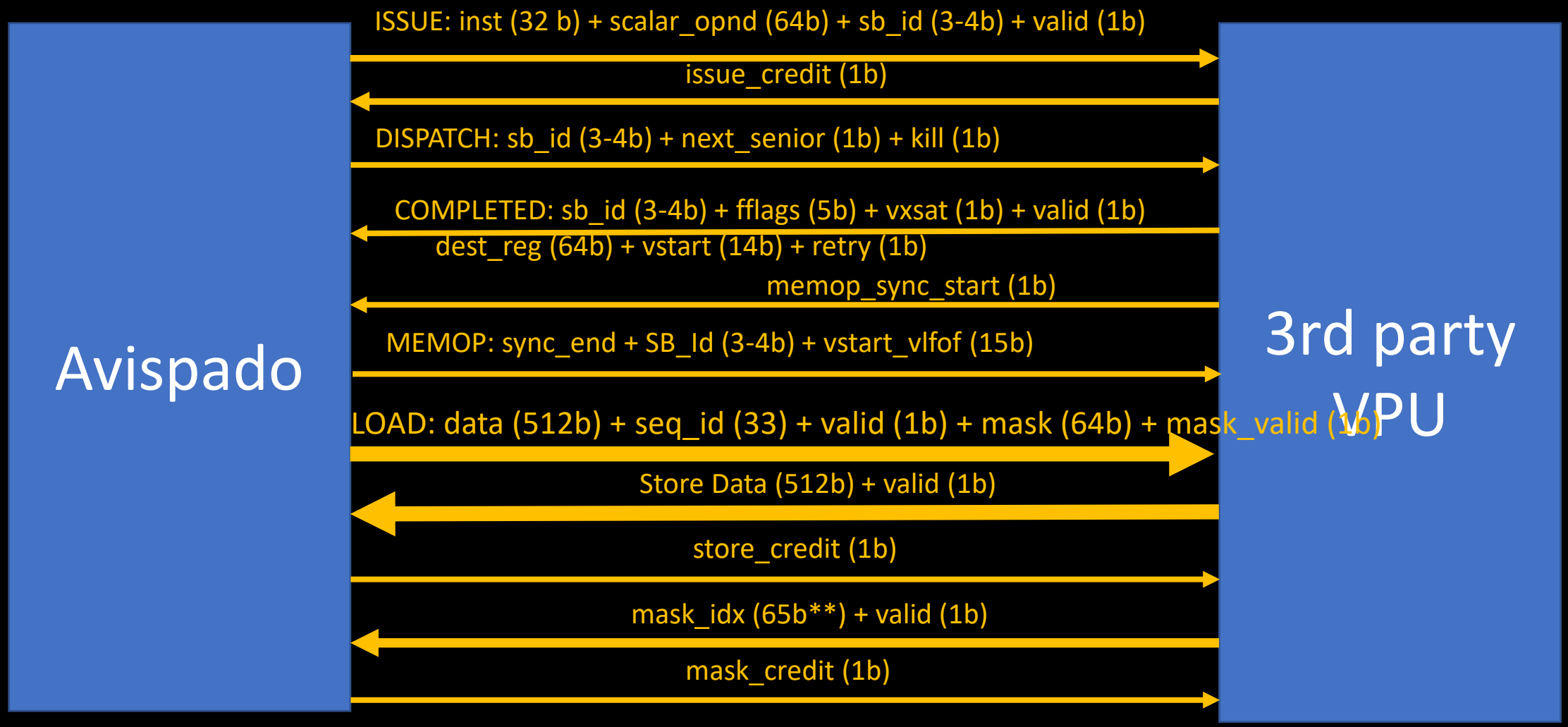
- Avispado Decodes the RISC-V Vector Specification
  - Including lmul, segmented loads
  - No vector atomics currently
- Ready for OOO support
  - Renaming
- Avispado executes the vector memory instructions
- Avispado connects to 3rd party VPUs using the Open Vector Interface

AVISPADO 220 with VPU

RISCV64GCV



OVI Interface: https://github.com/semidynamics/OpenVectorInterface



Summary

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VPU 1.0

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IP cores available for licensing

Thank you!

www.semidynamics.com

jobs@semidynamics.com (we are hiring!)